EMULEX IVC23E
CS23/CS04 E1 VAX INSTALLATION DIAGNOSTICS
USER'S GUIDE

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This diagnostic distribution kit contains one of the following diagnostic distribution media:

Emulex Part Number	Type of Media	Partial Contents
VX9960402	TU58 for 11/730, 11/750	EVM.EXE IVC23E.EXE
VX9960502	Floppy for 11/780	EVM.EXE IVC23E.EXE

This kit contains one or more of the following User's Manuals to document the programs contained on the distribution media:

Title: Emulex VAX Monitor (EVM) User's Guide
Publication Number: VX9950901

Title: Emulex MicroVAX Monitor (uEVM) User's Guide
Publication Number: VX9950910

Title: VAX Configuration Utility (IVV000) User's Guide
Publication Number: VX9950905

Title: CS23/E1 Communications Subsystem Technical Manual
Publication Number: CS2351001

Title: CS04/E1 Communications Subsystem Technical Manual
Publication Number: CS0451001

TABLE OF CONTENTS

LIST OF APPENDICES

LIST OF FIGURES

LIST OF TABLES

EMULEX PRODUCT WARRANTY

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Section 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

This manual is designed to serve as a guide for those using Emulex's IVC23E common installation diagnostic for Emulex Communication controllers CS23 and CS04 (emulations of Digital Equipment Corporation's DHU11 and DHV11, respectively). IVC23E runs under the control of Emulex VAX Monitor (EVM or MicroEVM).

These diagnostics are designed for use by qualified installers of Emulex equipment, and thus assume that the user has some knowledge of hardware configurations, VAX architecture and terminology, and interpretation of error messages and device register contents.

This document contains three sections:

Section 1	**General Description.** This section provides an overview of Emulex's IVC23E Installation Diagnostic, including its functions, distribution media, hardware and software requirements, and related documentation.
Section 2	**Operation.** This section describes the operation IVC23E Installation Diagnostic, including configuration and loading and start-up procedures.
Section 3	**Service.** This section explains Emulex service policies.

1.2 PRODUCT OVERVIEW

The ICV23E is a common installation diagnostic for Emulex communication controllers CS23E1 and CS04E1 which are emulations of Digital Equipment Corporation's DHU11 and DHV11 controllers, respectively.

The CS23/E1 is an asynchronous multiplexer that provides an interface between 32 full-duplex, asynchronous serial data communications channels (on one hex-wide DEC UNIBUS slot) and any processor that supports unibus devices, i.e., VAX 11/7XX series processors. CS23/E1 emulates two sixteen-line DEC DHU11s.

The CS04/E1 is an asynchronous communications multiplexer providing control of up to 64 full-duplex RS-232C serial channels on one quad-wide DEC LSI-11 Bus slot. The CS04/E1 emulates eight eight-line DEC DHV11's and requires only one CC04 controller installed in a LSI-11 bus slot. CS04/E1 controller is used with any processor that supports LSI-11 based devices, i.e, MicroVAX series computers.

IVC23E verifies that CS23/E1 controllers connected via unibus adapter or CS04/E1 controllers connected via LSI-11 bus to a VAX system are functioning correctly. It performs 25 different tests which ensure integrity and give the customer confidence in the performance of the CS23/E1 and CS04/E1 communications subsystems. Test descriptions appear in section 1.5.

1.3 LOOPBACK MODES

The operator has the ability to test CS23/E1 or CS04/E1 in internal or external loopback mode. If external loopback mode is selected, the appropriate loopback (wrap) connectors are placed on all selected lines and cabled in either a staggered or one-for-one fashion. Figure 1 shows staggered loopback cabling which requires the use of the staggered loopback connector (Emulex Part No. CU0411202). Figure 2 shows one-for-one cabling which requires the use of a one-for-one connector (Emulex Part No. CU0411203). The type of connectors used also depends upon the type of interface (RS-232, RS-422 or 20mA current loop) and the model of the distribution panel. In general CS04/E1 and CS23/E1 both use the above-described connectors. However, a CS23/E1 with a model CP25 distribution panel and RS422 interface requires a different set of connectors. A CS23/E1 with a model CP23 distribution panel and 20mA current loop interface also requires its own set of connectors. Appendix A provides schematics of the various connectors required by the IVC23E diagnostic. One staggered loopback connector (CU0411202) is provided by Emulex. Additional loopback connectors may be purchased from an Emulex technical representative or it is possible to build test connectors for any Emulex distribution panel by strapping a DB25S connector (shown in Appendix A).

CAUTION

IVC23E Test 16 (CTS/DCD To XON/XOFF Conversion Test) and IVC23E Test 18 (Modem Signal Test) function properly **only** if **standard** distribution panels are installed. A CS23/E1 requires either a standard CP22 or CP26 distribution panel. A CS04/E1 requires a standard CP34 distribution panel. Additionally, Test 16 runs only in external loopback mode using a one-for-one connector (CU0400203). Test 18 also runs only in external loopback mode, but it may use either the staggered connector (CU0400202) or the one-for-one connector.

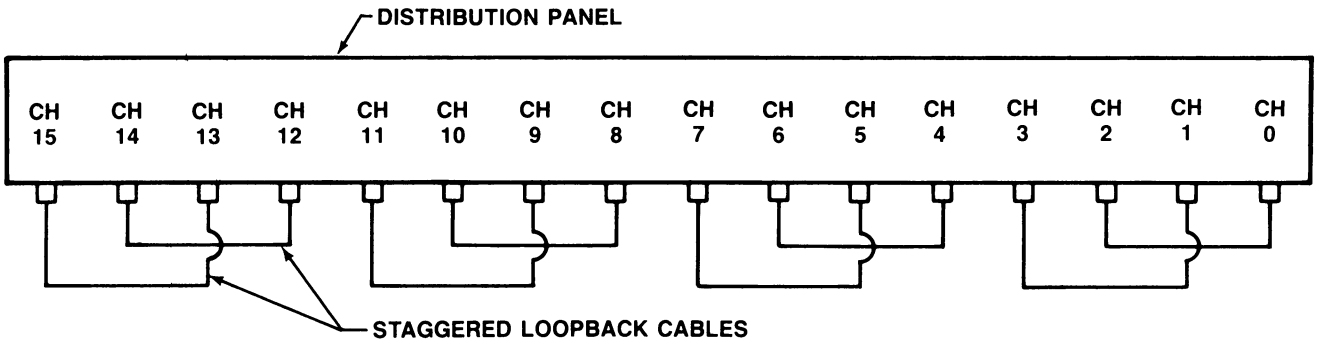

Figure 1-1. Staggered Loopback Connector Schematic

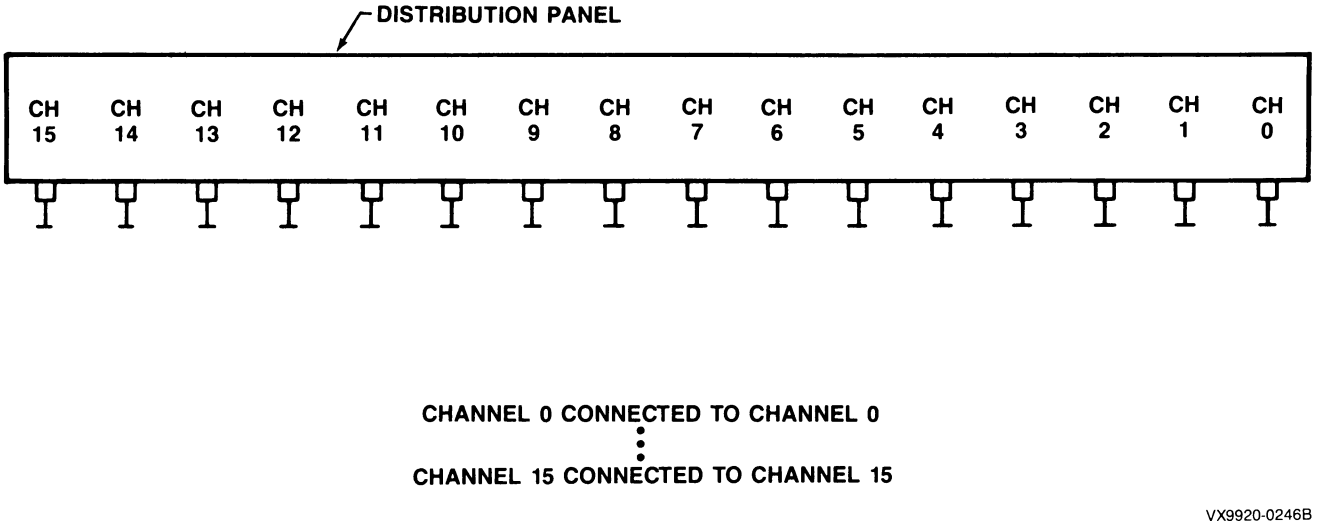

Figure 1-2. One-to-one Loopback Connector Schematic

Table 1-1 provides a ready reference of loopback mode options for the various tests.

Table 1-1. Loopback Mode Selection

TEST	LOOPBACK MODE		
	INTERNAL	EXTERNAL	
		One-for-one	Staggered
01	X	X	X
02	X	X	X
03	X	X	X
04	X	X	X
05	X	X	X
06	X	X	X
07	X	X	X
08	X	X	X
09			X
10	X	X	X
11	X	X	X
12	X	X	X
13	X	X	X
14	X	X	X
15	X	X	X
16		X	
17	X	X	X
18		X	X
19	X	X	X
20			X
21	X	X	X
22	X	X	X
23			X
24	X		
25	X		

1.4 COMPATIBILITY

1.4.1 HARDWARE

IVC23E runs in an offline environment on unibus based VAX 11/7xx series computer that have a CS23/E1 communications controller installed. It also runs on LSI-11 based MicroVAX series computers that have a CS04/E1 controller.

IVC23E requires the following hardware:

- DEC VAX-11/730, 11/750 or 11/780 **OR** MicroVAX I and II series computers

- Console terminal
- 256Kbytes of memory on any system configuration
- 1 to 32 CS23/E1 lines **OR** 1 TO 64 CS04/E1 lines

1.4.2 SOFTWARE

IVC23E standalone diagnostic runs under the control of Emulex VAX Monitor (EVM) or Emulex MicroVAX Monitor (uEVM).

1.5 DIAGNOSTIC TESTS

The following is a list of the tests performed by the IVC23E Installation Diagnostic:

TEST 01 - MASTER RESET/SELF-TEST, CHECK ROM.
TEST 02 - MASTER RESET/SKIP SELF-TEST
TEST 03 - SELF-TEST FORCED TO FAILURE TEST
TEST 04 - REGISTER ADDRESS TEST
TEST 05 - ID BIT TEST
TEST 06 - TX ENABLE/TX ACTION/TX ACTION FIFO
TEST 07 - TX/RX TEST, SINGLE CHARACTER MODE
TEST 08 - RX ENABLE/DATA VALID/DATA AVAILABLE TEST
TEST 09 - MAINTENANCE MODE TEST
TEST 10 - RX FIFO TEST
TEST 11 - INTERRUPT TESTS/BR LEVEL TEST
TEST 12 - DMA START, DMA ABORT TEST
TEST 13 - BYTE COUNT REGISTER TEST
TEST 14 - SPEED TEST
TEST 15 - XON/XOFF RECOGNITION TEST
TEST 16 - CTS/DCD TO XON/XOFF CONVERSION TEST (Uses only standard CP22, CP26 or CP34 panels)
TEST 17 - DMA ADDRESS/BYTE COUNT TEST
TEST 18 - MODEM SIGNAL TEST (Uses only standard CP22, CP26 or CP34 panels)
TEST 19 - OVERRUN DETECTION TEST
TEST 20 - PARITY GENERATION/DETECTION TEST
TEST 21 - FRAMING ERROR/BREAK BIT TEST
TEST 22 - EXERCISER TEST
TEST 23 - SPLIT SPEED TEST
TEST 24 - TERMINAL ECHO TEST
TEST 25 - TERMINAL DISPLAY TEST

There are three manual intervention tests included in IVC23E. These tests are the CTS/DCD TO XON/XOFF CONVERSION TEST (Test 16), TERMINAL ECHO TEST (Test 24) and TERMINAL DISPLAY TEST (Test 25). The CTS/DCD to XON/XOFF CONVERSION TEST verifies that the hardware level flow control translation to the software XON/XOFF control works properly. This test requires that the operator make the proper switch settings on the controller board as described in the Communications Subsystem Technical Manuals listed in the front matter on this manual. The

ECHO test echoes a Rx character from selected lines. The TERMINAL DISPLAY test transmits the familiar "barber-pole" pattern to selected lines. If the "No Operator" option is selected or if improper connectors are installed, IVC23E bypasses these tests.

IVC23E encounters the following kinds of errors: soft errors or preparation errors, hard errors or device fatal errors and system fatal errors. IVC23E reports preparation errors if the user has not properly prepared the Unit Under Test (UUT). For example, the CSR address may not correspond to the address on the controller, causing IVC23E to abort. In other cases of preparation error, only those tests which are affected by a particular error will abort and display error messages. A soft error is one that can possibly be recovered, such as a parity error. IVC23E retries an error three times before it becomes a hard error. Occurrence of a hard error allows the operator to manually abort the sequence at each occurrence with a **<CTRL C>**. If too many hard errors have occurred, IVC23E aborts the sequence itself and returns control to EVM. IVC23E declares system fatal errors if it receives unexpected status while executing system services. Such errors cause IVC23E to display normal versus abnormal status, abort and return control to EVM.

Following are descriptions of the tests performed by IVC23E:

1.5.1 TEST 01 - MASTER RESET/SELF-TEST, CHECK ROM CONTENTS

This test verifies that Bit 04 (Master Reset) in the CSR clears 0.5 seconds after setting. It verifies that self-test codes and status bits are normal. A hard error results if (a) Bit 4 does not clear in 0.5 seconds; (b) if the diagnostic fail bit is set, indicating self-test errors; or (c) if an unexpected self-test error code occurs.

1.5.2 TEST 02 - MASTER RESET/SKIP SELF-TEST

This test verifies that the Master Reset bit clears within .5 seconds after setting if the Skip Self-test sequence is selected. In the case of CS23/E1 Bit 04 is initially set in CSR. In the case of CS04/E1, IVC23E will wait 10ms for the firmware to write a pattern 125252(8) into the RAM. IVC23E then writes a pattern 052525(8) throughout the control registers (not the CSR) within the next four milliseconds. In both cases the test verifies the skip test code in ROM. A hard error occurs if (a) UUT is too short (10ms) or too long (50ms), causing the test to skip or to fail to complete Skip Self-test; (b) if diagnostic fail bit is set indicating an error; (c) if bit RX.AVAIL is clear and bit RX.VALID is set after self-test codes are read; or (d) if Skip Self-test codes are not as expected.

1.5.3 TEST 03 - SELF-TEST FORCED TO FAILURE TEST

This test verifies that the self-test reports errors correctly when it is forced to fail and that the diagnostic fail bit goes to both

active and inactive states. A hard error occurs if (a) self-test fails to complete or (b) self-test does not detect a forced error.

1.5.4 TEST 04 - REGISTER ADDRESS TEST

This test verifies that the registers can be uniquely addressed. The test writes patterns into the registers, and then reads them back. If all data is not unique (except undefined bits), then an error condition exists. The test also verifies that word and byte accesses work properly. Read or write only registers, or registers that cause unwanted action are not included. A hard error occurs if (a) word or byte read is not the same as was written or (b) a read/modify/write word or byte read is not the same as was written.

1.5.5 TEST 05 - ID BIT TEST

For the CS23/E1 (DEC DHU emulation) Bit 08 (DHUID) in the STAT register (BASE+6) is always set. For the CS04/E1 (DEC DHV emulation) Bit 08 is always clear. A hard error occurs if (a) bit 08 is clear for a DHU emulation or (b) bit 08 is set for a DHV emulation.

1.5.6 TEST 06 - TX ENABLE/TX ACTION/TX ACTION FIFO

This test verifies that if a data word is written without setting Bit 15 (TX.ENABLE) in TBUFFAD2, no TX actions are generated. A hard error occurs if (a) the respective bit settings are unexpected when verified after each test sequence (TX.ACTION, TX.ENABLE); (b) the DMA error bit is set; or (c) bit settings are on unexpected lines.

1.5.7 TEST 07 - TX/RX TEST, SINGLE CHARACTER MODE

This test verifies that the UUT will transmit RX data correctly in single character mode. A hard error occurs if data is erroneous.

1.5.8 TEST 08 - RX ENABLE/DATA VALID/DATA AVAILABLE

This test verifies that (a) RX.DATA.AVAILABLE (Bit 07 of CSR) and RX.DATA.VALID bits do not set when a character is transmitted with a cleared RX.ENABLE (Bit 02 of LNCTRL) and (b) that they do set when a character is received with a set RX.ENABLE bit. A hard error occurs if (a) RX.ENABLE is set after reset; (b) there is incorrect status for RX.AVAIL and RX.VALID when in internal loop at each test step; (c) there is improper status for RX.AVAIL and RX.VALID for lines other than current one at each step; (d) there is an error in received data; or (e) data is received on an unexpected line.

1.5.9 TEST 09 - MAINTENANCE MODE TEST

This test requires staggered loopback connectors and verifies that the maintenance modes are working correctly. A hard error error occurs if (a) the maintenance mode did not initialize to normal mode; (b) if a line failed to set to internal maintenance mode; (c) if internal mode set for line other than current one; (d) if RX.AVAIL and RX.VALID bits are not correct for transmission on internal loop; (e) if data received with errors (f) if data received not the same as data transmitted or (g) or if data received is in error and/or on an unexpected line.

1.5.10 TEST 10 - RX FIFO TEST

This test verifies that the FIFO locations can be uniquely addressed from the UNIBUS. The FIFO is filled with 256 unique bytes of data and then checked for data integrity. A hard error occurs if (a) data fails to be transmitted; (b) RX.AVAIL clears before RX FIFO is empty; (c) data is received with errors; (d) data received is not same as data transmitted; (e) data is received on unexpected line.

1.5.11 TEST 11 - INTERRUPT TESTS/BR LEVEL TEST

This test verifies that RX and TX interrupts work correctly at the BR level set in the UUT. A hard error error occurs if (a) an interrupt enable bit fails to set; (b) if a reset fails to complete; (c) if Master Reset clears enable bits; (d) if unibus initiate does not clear these bits; (e) if interrupts occurred with interrupt disable; (f) if unexpected interrupts occurred; (g) if interrupt occurred at wrong vector; (h) if interrupt occurred at BR level other than one set in the UUT; (i) or if RX or TX interrupts failed to occur.

1.5.12 TEST 12 - DMA START, DMA ABORT TEST

This test verifies that each DMA start bit will initiate a DMA transfer on a line, that it can be aborted and resumed, and that DMA abortions and completions cause interrupts. A hard error occurs if (a) timeout occurs before DMA is completed or if timeout fails to cause an interrupt; (b) if there are DMA errors; (c) if the DMA start bit is still set after completion; (d) if aborted DMAs are not aborted within two seconds; (e) if DMA abort did not abort DMA; (f) if DMA abort did not cause an interrupt; (g) if a DMA abort did not clear DMA start bit; (h) if a DMA error sets after DMA abort; (i) if DMA did not interrupt upon restart; (j) if DMA error bit sets after restart; (k) or if DMA did not cause TX.ACTION bit to set.

1.5.13 TEST 13 - BYTE COUNT REGISTER TEST

This test verifies that the byte count registers work properly. The test tallies the number of bytes received for each line and checks to

see if it is the same number as transmitted. A hard error occurs if (a) timeout occurs before DMA is interrupted or (b) if number of bytes received is incorrect.

1.5.14 TEST 14 - SPEED TEST

This test transmits characters at all speeds on all lines in internal loopback mode. This test uses DMA to send characters. A hard error occurs if (a) line speed is not initialized to 9600 bps; (b) if DMAs could not be aborted within two seconds; (c) if not enough characters were transmitted for current speed.

1.5.15 TEST 15 - XON/XOFF RECOGNITION TEST

This test verifies that XON/XOFF control works properly. A hard error occurs if (a) bits I.AUTO, O.AUTO, and FORCE XOFF fail to set; (b) if INIT does not clear these three bits; or (c) if any of the test steps result in error.

1.5.16 TEST 16 - CTS TO XON/XOFF CONVERSION TEST

This test verifies that the hardware level flow control translation to the software XON/XOFF control works properly. It requires manual intervention and operates only in external loopback mode using a one-to-one (wrap-around) loopback connector. In order for this test to operate properly, use only standard CP22 or CP26 (for the CS23/E1) or CP34 (for the CS04/E1) distribution panels (NO JUMPERS INSTALLED). **Enable the Hardware Flow Control Switch settings before performing this test.** To use the CS23/E1 flow control options, refer to Section 4.4.5.7, Hardware Flow Control, of the CS23/E1 Communications Subsystem Technical Manual. To use the CS04/E1 flow control options, refer to Sections 4.3.3.6 and 4.3.3.7 of the CS04/E1 Communications Subsystem Technical Manual. Also refer to Table 4-5, CP34 Option Switch Settings/Factory Configuration. After completing this test, disable the switch settings so that IVC23E may properly perform any of the other tests. By reading firmware RAM, IVC23E determines whether the hardware level flow control is enabled, its mode (DCD or CTS, transparent or non-transparent), and whether or not a 16-channel panel is installed. The test runs on a per channel basis. IVC23E queries the operator for emulation and line number to be tested. Refer to the appropriate Communication Subsystem Technical Manual listed in this manual's front matter for information concerning the options for enabling the level flow control.

1.5.17 TEST 17 - DMA ADDRESS/BYTE COUNT TEST

This test verifies the ability of the device to correctly increment addresses and byte counts. It verifies a DMA of 2000 bytes of decrementing data for absence of errors. This test is performed on only one line, since the DMA logic is common to all lines, and the

memory containing the lines' addresses and byte counts has been checked by the self-test. The test repeats until all address lines have been tested. A hard error occurs if (a) timeout occurs before DMA is completed; (b) if there are DMA errors; (c) if not all data is received; (d) if data is received with errors; (e) if data received is not same as data transmitted.

1.5.18 TEST 18 - MODEM SIGNAL TEST

This test verifies various modem related signals and states. A hard error occurs if at each test step the bits RTS, RING, DTR, DSR, DCD, CTS etc. show incorrect status. In order for this test to operate properly, use only standard CP22 or CP26 (for the CS23/E1) or CP34 (for the CS04/E1) distribution panels (NO JUMPERS INSTALLED).

1.5.19 TEST 19 - OVERRUN DETECTION TEST

This test verifies that the unit under test receives the maximum number of characters without causing an overrun error, and that a character in excess will cause overrun. A hard error occurs if (a) an overrun error occurred unexpectedly (b) an overrun error bit is not set; (c) or if data with overrun is not a null character.

1.5.20 TEST 20 - PARITY GENERATION/DETECTION TEST

This test verifies that parity works correctly (odd,even) and that parity errors are reported. This test works in staggered loopback only. A hard error occurs if parity error is not indicated when the transmit parity setting is different from the receive parity setting.

1.5.21 TEST 21 - FRAMING ERROR/BREAK BIT TEST

This test verifies that forced framing errors are reported correctly. Staggered loopback mode is required to run the framing error test. Break bit test will run regardless of the loopback mode selection. A hard error occurs if (a) no frame error occurs when transmit data size is different from receive data size or (b) a set break bit does not cause a framing error.

1.5.22 TEST 22 - EXERCISER TEST

This test simultaneously enables all lines for transmission at 9600 bps. The test uses 1024 byte buffers for transmission and reception with a format of eight bits, no parity, and one stop bit. A hard error occurs if (a) timeout occurs before DMA completes; (b) if there are DMA errors; (c) if all the data is not received; (d) data is received with errors; or (e) the data received is not the same as the data transmitted.

1.5.23 TEST 23 - SPLIT SPEED TEST

This test verifies that the split speed operations work correctly. This test works in staggered loopback only. A hard error occurs if (a) the Tx/Rx speed did not set to correct speed; (b) data is in error; (c) data on adjacent line is not the same as was transmitted; (d) or less data is received than expected.

1.5.24 TEST 24 - TERMINAL ECHO TEST

This test requires manual intervention by the operator and connection of a terminal to the line(s) under test. The test echoes back all the characters typed on the terminal. It queries the operator as to which line to echo the data. This allows isolation of the direction in which a line may be failing. This test will run until interrupted by a **CTRL C** from the system console terminal. Error messages occur if (a) received characters are in error or (b) if there are timeouts during transmission.

1.5.25 TEST 25 - TERMINAL DISPLAY TEST

This test requires manual intervention by the operator and connection of a terminal to the line(s) under test. The test transmits the contents of a buffer filled with a rotating ASCII pattern (barber pole) to selected lines (by selection of line masks). This isolates the direction in which a line may be failing. This test will run until interrupted by a **CTRL C** from the system console terminal. An error message occurs if (a) there are transmission errors or (b) if there are timeouts during transmission.

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Section 2
OPERATION

2.1 OVERVIEW

This section includes IVC23 load and start procedures, diagnostic test definitions, operating instructions, and sample user dialog.

User input appears in **bold** type to distinguish it from diagnostic monitor prompts and program messages. In text the symbol **<return>** indicates the carriage return key.

As used in prompts, the abbreviation DEC signifies decimal radix rather than Digital Equipment Corporation. Prompts for numeric parameters include the minimum and maximum acceptable values, followed by the default value in parentheses. The following example illustrates these conventions:

```
Enter emulation number [DEC - 0,1,(0)]>>>1<return>
```

For information regarding EVM command syntax, see the EVM User's Guide.

2.2 LOAD AND START PROCEDURES

2.2.1 LOAD PROCEDURE

The procedure used to invoke EVM varies from one VAX system to another. For a description of EVM bootstrapping procedures, see the EVM User's Guide.

After the EVM> prompt appears on the screen, type the following:

```
EVM>LOAD IVC23E.EXE<return>
```

The LOAD statement may be followed by a SET CONFIGURATION statement, the content of which depends upon the VAX system being used. Sample configure statements for the VAX-11/730, 11-750, and 11-780 appear in the following subsections.

2.2.1.1 Sample Configure Statement For VAX-11/730

The following example refers to a VAX-11/730 with one CS23/E1 at CSR address 760340 and vector 300:

```
EVM>LOAD IVC23E.EXE<return>
EVM>SET CONFIG/CSR:760340/VECTOR:300<return>
EVM>SET FLAG/NO_OPER   (Enter this statement to skip manual
intervention tests.)
EVM>CLEAR FLAG/NO_OPER (Enter this statement to run manual
intervention tests.)
```

2.2.1.2 Sample Configure Statement For VAX-11/750

The following example refers to a VAX/11-750 with one CS23/E1 at CSR address 760340, vector 300, UNIBUS adapter UBA0 (base address FC0000), and device BR level 4:

```
EVM>LOAD IVC23E.EXE<return>
EVM>SET CONFIG/CSR:760340/VECTOR:300/ADAPTER:0/BR:4/UBR:5<return>
EVM>SET FLAG/NO_OPER   (Enter this statement to skip manual
intervention tests.)
EVM>CLEAR FLAG/NO_OPER (Enter this statement to run manual
intervention tests.)
```

In the preceding statement, /ADAPTER needs to be specified only if it is other than UBA0: (the default). Acceptable values for ADAPTER are 0 or 1:

```
ADAPTER #0      UBA0, FC0000
ADAPTER #1      UBA1, F30000
```

BR needs to be specified only if the BR level of the UNIBUS adapter is other than 4. Acceptable values for BR are 4 through 7. Four is the default for UNIBUS adapters.

UBR needs to be specified only if the device BR level is other than 5. Acceptable values for UBR are 4 through 7. Five is the default for all Unibus devices.

2.2.1.3 Sample Configure Statement For VAX-11/780

The following example refers to a VAX-11/780 with the same configuration as the 11/750 in the previous example. UBA0 corresponds to TR 3:

```
EVM>LOAD IVC23E.EXE<return>
EVM>SET CONFIG/CSR:760340/VECTOR:300/TR:3/BR:4/UBR:5<return>
```

In the preceding statement, /TR is optional and needs to be specified only if it is other than TR 3 (UBA0). Valid values for this parameter are 3 through 6, with 3 the default:

```
TR  3     UBA0, 20100000
TR  4     UBA1, 20140000
TR  5     UBA2, 20180000
TR  6     UBA3, 201C0000
```

BR needs to be specified only if the BR level of the UNIBUS adapter is other than 4. Acceptable values for BR are 4 through 7. Four is the default for UNIBUS adapters.

UBR needs to be specified only if the device BR level is other than 5. Acceptable values for UBR are 4 through 7. Five is the default for all Unibus devices.

2.2.1.4 Sample Configure Statement for MicroVAX Series Computers

uEVM>**LOAD IVC23E.EXE<return>**
uEVM>**SET CONFIG/CSR:760340/VECTOR:300<return>**
uEVM>**SET FLAG/NO_OPER** (Enter this statement to skip manual intervention tests.)
uEVM>**CLEAR FLAG/NO_OPER** (Enter this statement to run manual intervention tests.)

2.2.2 START PROCEDURE

2.2.2.1 Sample Diagnostic Program Run

After entering the LOAD and SET CONFIGURATION statements to load IVC23E via EVM or uEVM and configure it for the system it will be running in, the operator may start the tests as shown in the following example. For a detailed description of the start procedure see section 2.2.2.2. The DHV11 emulation runs under uEVM, and the operational sequence is the same.

CAUTION

Ordinarily, the hardware flow control switch settings are not enabled. **To ensure that IVC23E performs properly, these switch settings must NOT be enabled when running the IVC23E diagnostic tests.** The **only** exception to this rule is Test 16. **Test 16 requires that the hardware flow control switch settings be enabled.** Refer to the CS04/E1 or the CS23/E1 Communication Subsystems Technical Manuals for complete information on hardware flow control switch settings.

EMULEX VAX MONITOR REV no. VAX-11/7XX DD-MMM-YYYY TIME

EVM> Please enter date and time DD-MMM-YYYY HH:MM:SS 31-JAN-1986 9:9:0

31-JAN-1986 09:09:00<return>

EVM>**LOAD IVC23E.EXE<return>**

EVM> **SH C<return>**

CONFIGURATION PARAMETERS FOR UNIT SELECTED ARE:
BR = 5
ADAPTER # = 0
CSR = 760060
VECTOR = 320
UBR = 5
DRIVE # = 0

```
EVM>  ST<return>

EMULEX CS23/CS04 COMMUNICATION CONTROLLER DIAGNOSTICS REV X1.0
    31-JAN-1986  09:09:00

Configuration and Default Parameters
Controller Type = 1  (CS04 = 0, CS23 = 1)
Number of Controllers = 2(D)
Number of emulations = 4(D)
Emulation Mask = F(X)
Default Baudrate = 9600(D)
Default Looptype = S - (I=Internal, S=Staggered,E=External)
Following line masks and parameters are selected for each Emulation:

-------------------------------------------------------------------------
Emulation   Line Mask   RX Vec    Max Lines     LFC Mode     LFC Linemask
-------------------------------------------------------------------------
    1(D)      0FFF(X)     320(O)    12(D)        1(X)          0000(X)
    2(D)      0FFF(X)     330(O)    12(D)        1(X)          0000(X)
    3(D)      0FFF(X)     360(O)    12(D)        1(X)          0000(X)
    4(D)      0FFF(X)     370(O)    12(D)        1(X)          0000(X)

Do you wish to alter the emulation or line masks?
[Y,N,(N)]>>>Y<return>

Enter line selection mask for emulation 1 :
    [Hex - 0,FFF,(FFF)]>>> <return>

Enter line selection mask for emulation 2 :
    [Hex - 0,FFF,(FFF)]>>> 0<return>

Enter line selection mask for emulation 3 :
    [Hex - 0,FFF,(FFF)]>>> 0<return>

Enter line selection mask for emulation 4 :
    [Hex - 0,FFF,(FFF)]>>> 0<return>

Numeric code for valid Baud rates:
    num  bps       num  bps       num  bps       num  bps
    0    50        1    75        2    110       3    134
    4    150       5    300       6    600       7    1200
    8    1800      9    2000      10   2400      11   4800
    12   7200      13   9600      14   19200     15   38400

Enter the numeric code for Baud rate desired:  [DEC - 1,15,(13)]>>>
    <return>

Numeric code for valid Loop Types:  1=Internal, 2=External,
3=Staggered)

Enter Numeric Code for loop type desired  [DEC - 1,3,(3)]>>>3<return>
```

```
Operator selected masks and parameters
Number of Emulations = 4(D)
Emulation Mask = F(X)
Baudrate = 9600
Looptype = E - (I=Internal,S=Staggered,E=External)

Following line masks are selected for each Emulation:
```

Emulation	Line Mask	RX Vec	Max Lines	LFC Mode	LFC Linemask
1(D)	0FFF(X)	320(O)	12(D)	1(X)	0000(X)
2(D)	0000(X)	330(O)	12(D)	1(X)	0000(X)
3(D)	0000(X)	360(O)	12(D)	1(X)	0000(X)
4(D)	0000(X)	370(O)	12(D)	1(X)	0000(X)

```
----> BEGINNING OF PASS 1

Test # 1  Master Reset/Selftest, Check ROM Contents
                                  .
                                  .
                                  .
Test # 25  Terminal Display Test
```

2.2.2.2 Detailed Startup Description

This section describes in greater detail each of the fields that the IVC23E diagnostic displays during startup. EVM provides standard services that will prompt RADIX, minimum, maximum, (default). Operator input of a **<return>** will assume default value.

EVM> ST
Enter ST at the EVM prompt to begin test execution. There are several modifiers that may also be entered at this time, such as **vector, CSR, test numbers, number of passes,** etc. Reference the EVM or uEVM User's Guides for a complete lists of modifiers.

Emulex CS23/CS04 Communication Controller Diagnostics REV X1.0
This identifying header displays the program name and its revision level.

Configuration and Default Parameters
ICV23E identifies the controller type and lists the number of emulations, emulation mask, line mask, baud rate and type of loopback mode. The default values assumed are best guess values. The user may override or select the current default values as he wishes. Default values, if never previously overridden, are the original program default values. However, if the user has subsequently altered the values, then IVC23E derives the default values from the last values entered by the user.

Do you wish to alter the emulation or line masks ?
The diagnostic first displays a list of all emulations and the current corresponding line masks, RX vectors, the maximum number of lines, and the LFC switch. It then asks the user if he wishes to change the current test parameters and line masks. Responding affirmatively (Y) to this prompt causes the program to prompt for line masks for all selected emulations. If there is only one CS23/E1 controller, then IVC23E will create a mask of three (hex) to include two emulations. IVC23E will in addition assign a default line mask of hex FFFF for 16 lines per DHU emulation. In the case where there is only one CS04/E1 controller, IVC23E will create a mask of hex FF for eight emulations. For DHV emulation, the default line mask is hex FF for eight lines. If you need to override the defaults for both emulation and line selection, answer **Y**. If this is not the first run, then IVC23E will prompt with default values from the previous run. A carriage return will select the default values. By use of the emulation and line masks, the operator can isolate one line or a group of lines for testing. The maximum line mask per emulation is eight lines for a CS04/E1; 16 lines for a CS23/E1; and 12 lines for a CS23/E1 with a CP26 distribution panel.

Numeric code for valid baud rates:
Sixteen possible baud rates are listed and selectable by code number. Enter the desired baud rate at the prompt which follows.

Numeric code for valid loop types: (1=Internal, 2=External, 3=Staggered)
Select the appropriate loop type at the prompt which follows.

Operator selected masks and parameters
The diagnostic lists the number of emulations, emulation mask, baud rate and loopback mode selected.

Following line masks are selected for each emulation:
The diagnostic lists the emulation number and corresponding line mask that has been selected before commencing the first pass of tests.

----> BEGINNING OF PASS 1
As each test is successfully completed, IVC23E lists the test number, test name, the date and time. If IVC23E encounters an error situation it also identifies the type of error and lists related error data.

2.2.2.3 Sample Error Message

The following example represents a typical error reporting message displayed by IVC23E. This particular example illustrates the kind of error reporting that would occur due to a faulty connector or cable on a CS23/E1.

```
Test # 22  Exerciser Test   21-FEB-1986  09:28:34

DMA Incomplete - Not all lines interrupted or aborted

Received int mask: 07FF(X)
Expected int mask: 0FFF(X)
XOR int mask     : 0800(X)
PASS #1  TEST  # 22 HARD ERROR
Timeout occurred before DMA completed

Emulation = 1(D), Test Line = 0(D), Current line = 0(D)

Test Line Registers

CSR:          4A40(X)        ; TXIE,TXLINE=10(D),RXIE,INDEXREG=0(D)
RBUF:         0000(X)        ; RXLINE=0(D),RXCHAR=0(X)
LPR:          BB38(X)        ; TXSPEED=11(D),RXSPEED=11(D),PARITYENB,
                               CHARLGTH=3(D),DIAGCODE=0(D)
STAT:         01(X)          ; ID
FIFOSIZE:     40(X)          ; FIFOSIZE=40(X)
LNCTRL:       0084(X)        ; MAINT=2(D),RXENA
TBUFFAD1:     0400(X)        ; TXADR1=400(X)
TBUFFAD2:     8000(X)        ; TXENA,TXADR2=0(X)
TBUFFCT:      0000(X)        ; TXBUFFCT=0(X)
```

An error message reports the occurrence of an unexpected event in accordance with the steps being executed during the test. In the above example Test 22 has encountered a line that did not complete DMA and, therefore, timed out on interrupt. IVC23E displays the received line mask and the expected line mask (those lines that should have interrupts due to DMA completion). The XOR function identifies those lines which timed out. The diagnostic identifies the current emulation, the line being tested and a line other than the test line which was indexed during the test. The diagnostic displays the contents of the Test Line registers which are identified by the mnemonics in the left-hand column. The respective bit settings and radix for the contents of each register are also displayed. Refer to the appropriate Communications Subsystem Technical Manual listed in the front matter for bit definitions and functions.

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Section Three
SERVICE

Emulex thoroughly tests its products. If IVC23E indicates a malfunction of the CS23 or CS04 controllers or if you have trouble with IVC23E itself, contact Emulex or its representative.

In the continental United States, Alaska and Hawaii contact:

Emulex Technical Support
3545 Harbor Boulevard
Costa Mesa, CA 92626
(714) 662-5600 TWX 910-595-2521
(800) 854-7112 Outside of California Only

Outside the United States, contact the distributor from whom the product was initially purchased.

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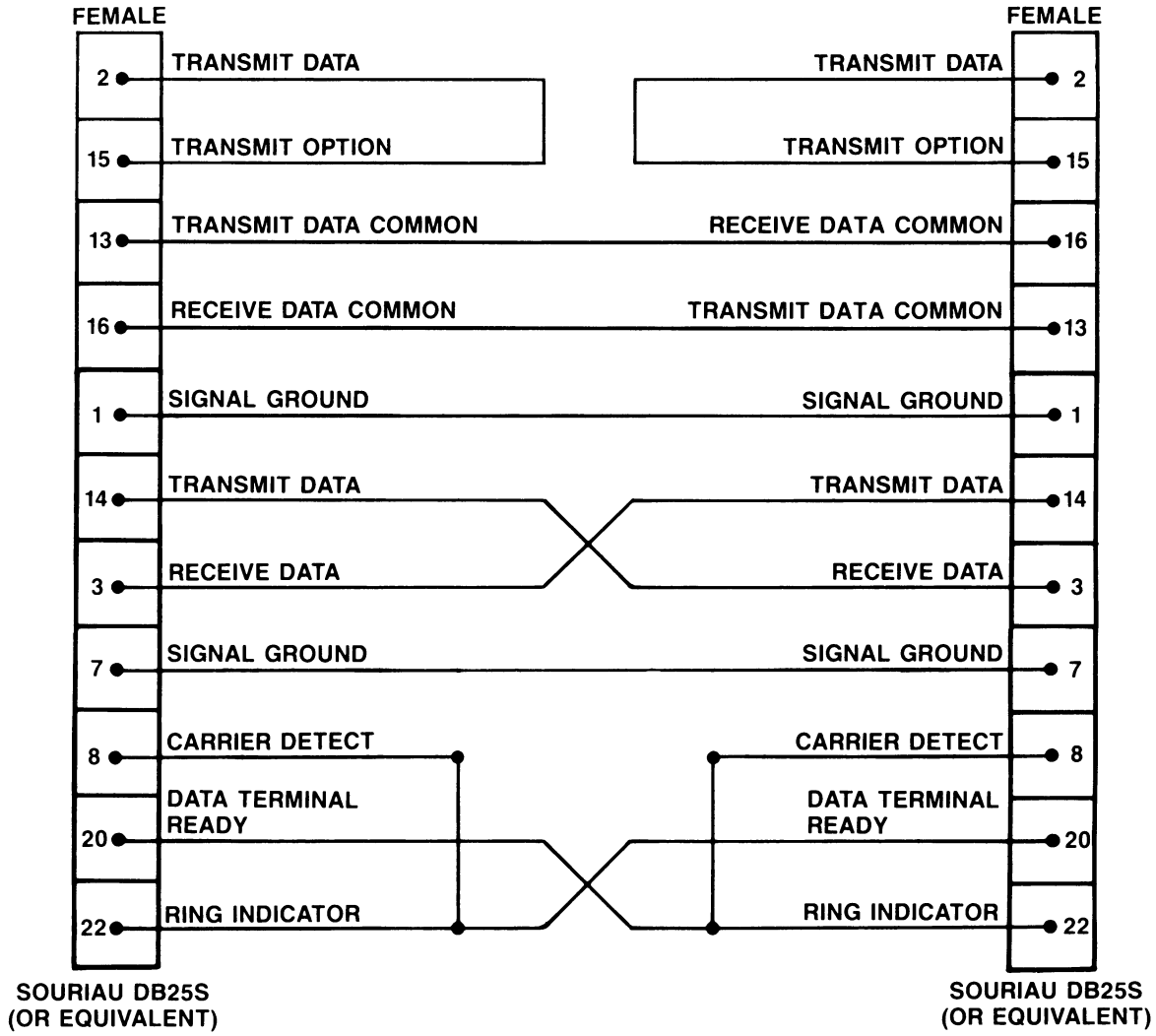
The following figures illustrate the various types of test connectors used for the CS04 and CS23 communication controllers. The type of connector used is determined by the type of interface (RS-232, RS-422 or 20mA current loop) and the model number of the distribution panel (CP22, CP23, CP25, or CP26). Instructions for building the appropriate connectors are contained in the distribution panel technical manuals. Distribution panels CP22, CP24, CP25, and CP26 all use the DHV11 staggered or loopback connectors unless they have an RS-422 interface. In that case they require the DHU11 RS-422 staggered or wrap-around connectors. Distribution panel CP23 requires the DHU11 20mA staggered or wrap-around connectors.



EMULEX PART NUMBER CU0411202

VX9920-0930

Figure A-1. DHU11 RS-422 Staggered Loopback Connector

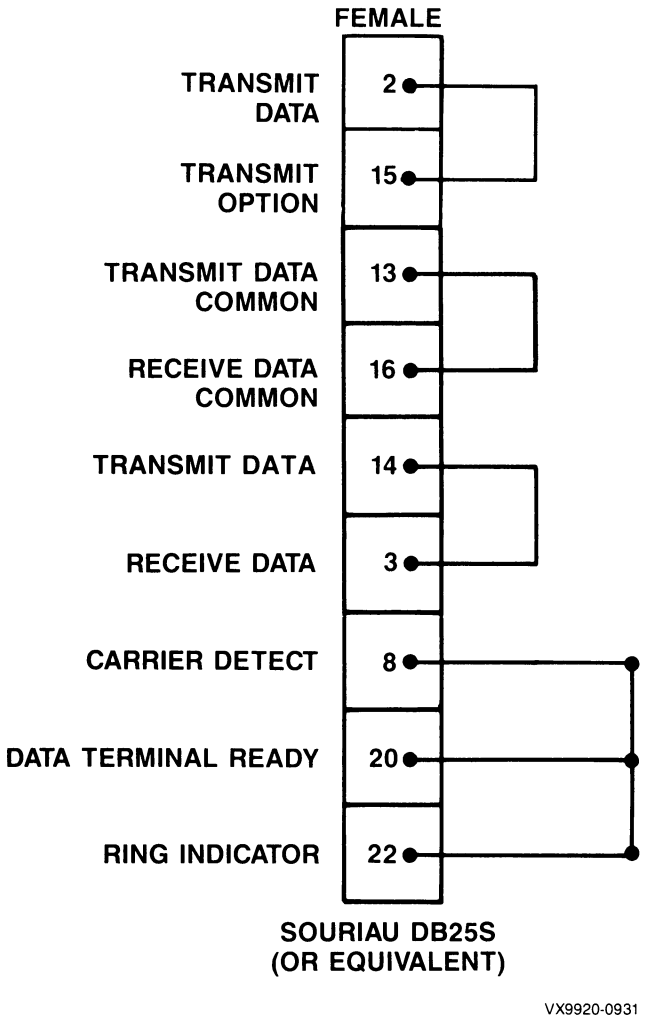


Figure A-2. DHUl1 RS-422 Wrap-around Loopback Connector

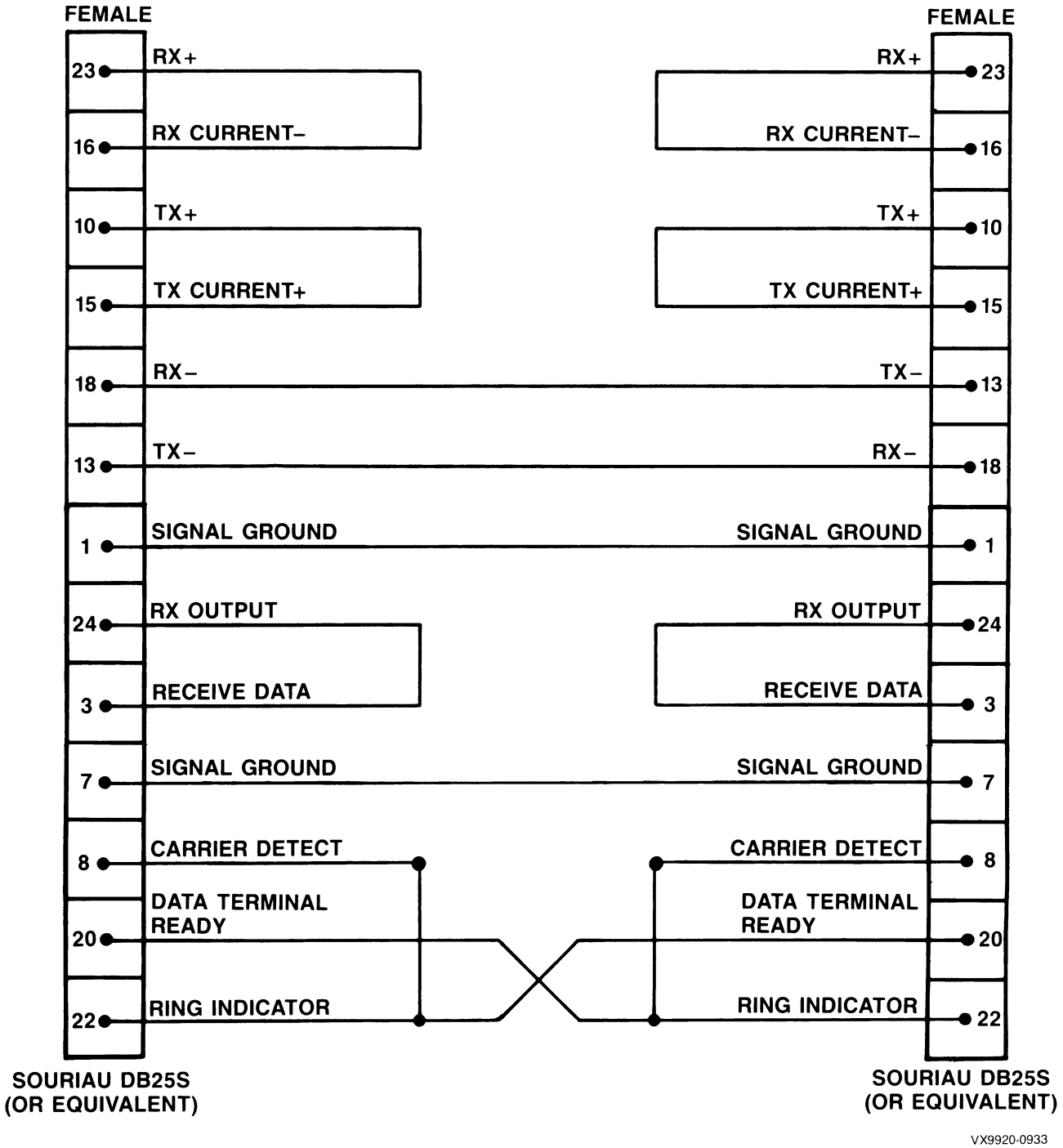


Figure A-3. DHUl1 20mA Current Loop Staggered Connector

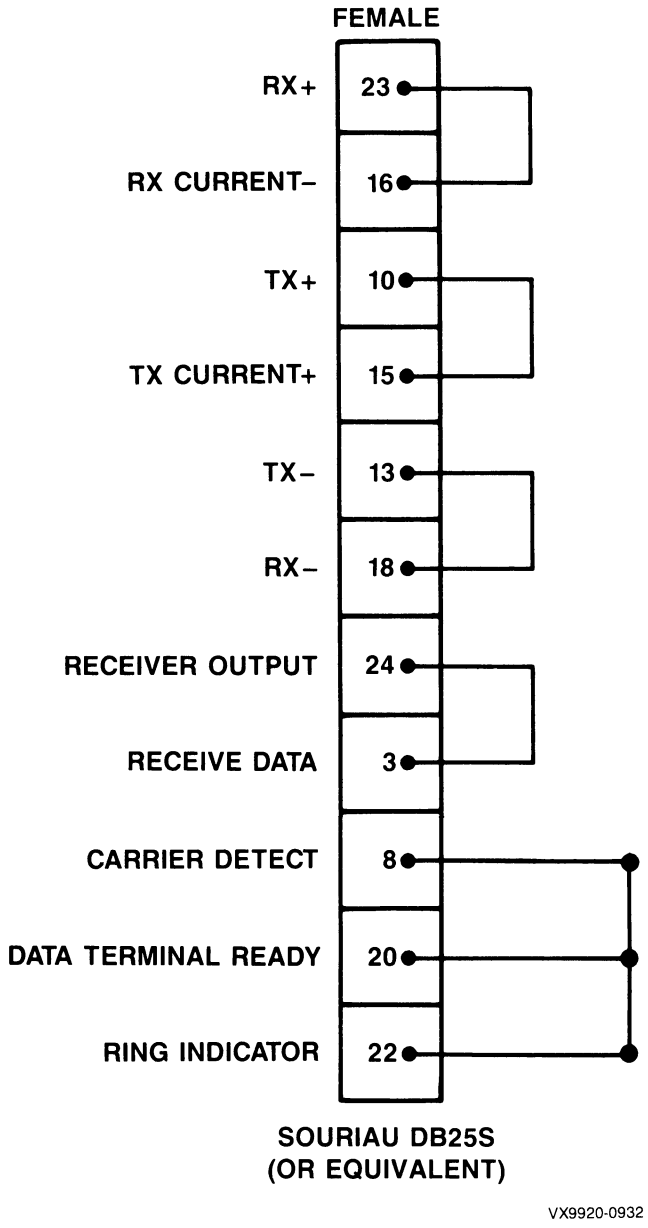


Figure A-4. DHUll 20mA Current Loop Wrap-around Connector

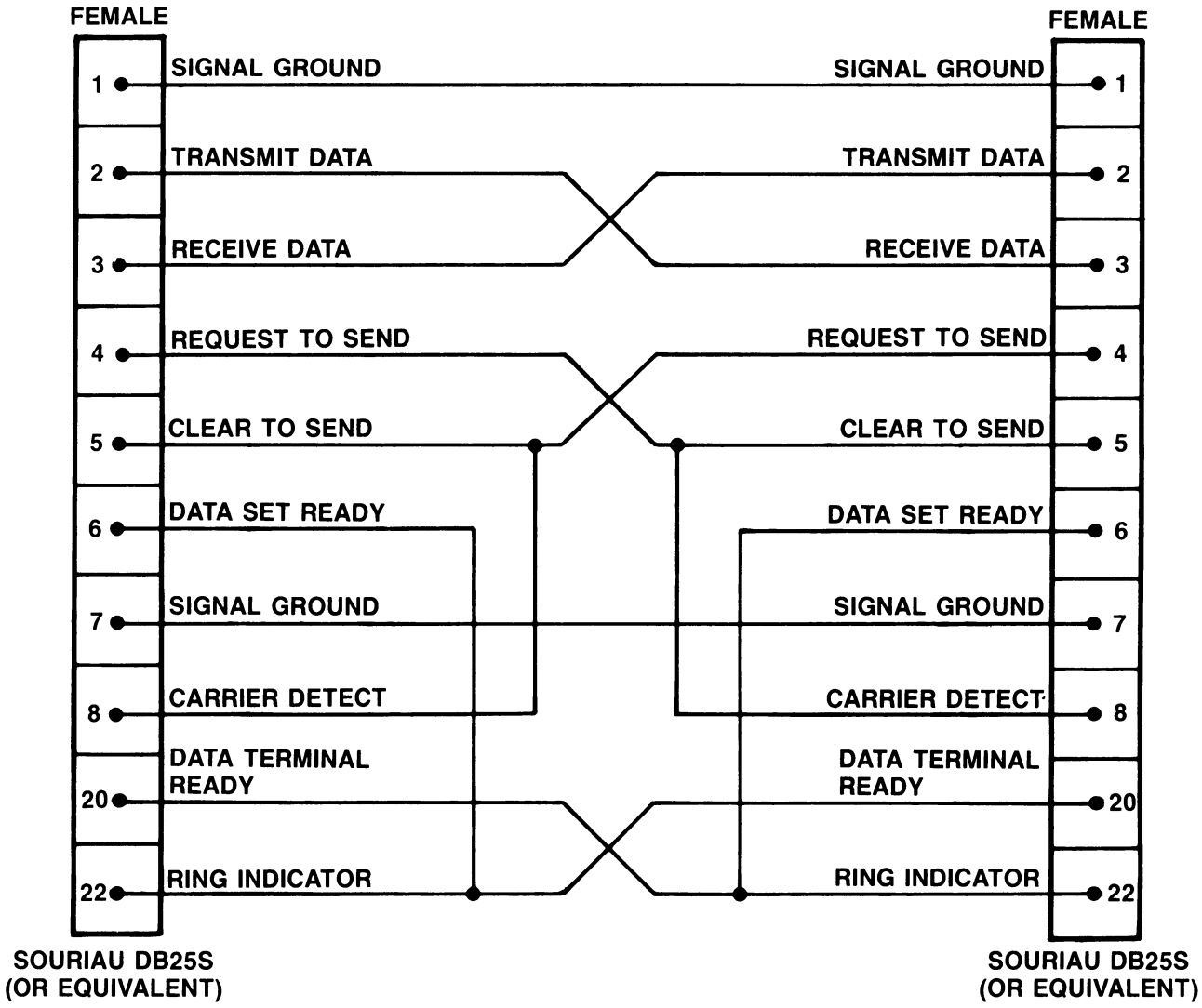


Figure A-5. DHV11 Staggered Loopback Connector

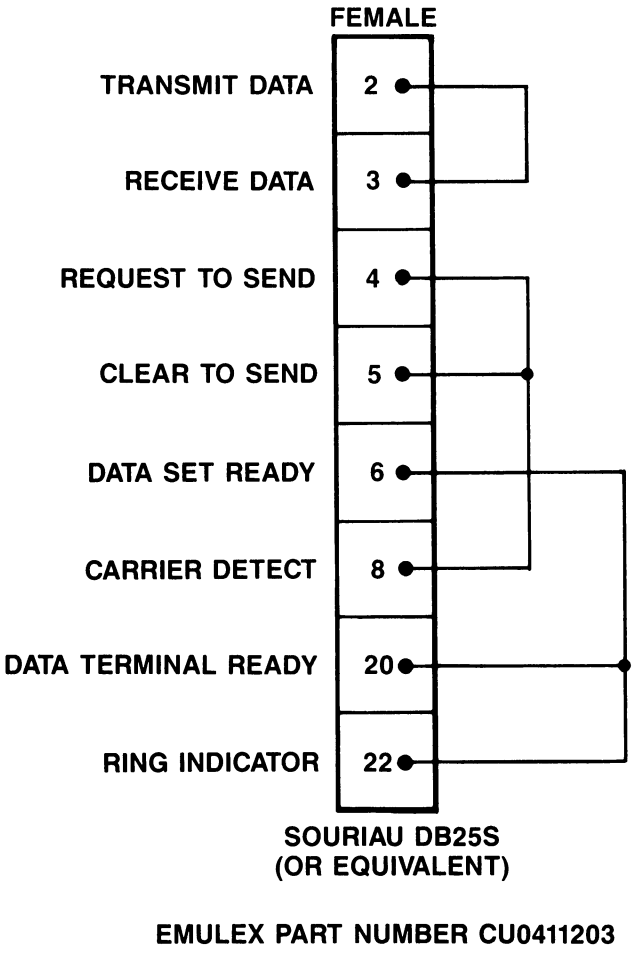


Figure A-6. DHV11 Wrap-around Loopback Connector